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November 27, 2000

BOX PATENT APPLICATION  
Assistant Commissioner for Patents  
Washington, D.C. 20231

Re: Junichi KOKUDO  
HIGH SPEED TIMESLOT ASSIGNMENT UNIT  
AND METHOD FOR A TDMA  
COMMUNICATION SYSTEM  
Our Ref. Q61990

Dear Sir:

Attached hereto is the application identified above including 12 sheets of the specification, claims, 3 sheets of informal drawings, and a copy of the executed Declaration and Power of Attorney. The Assignment will be filed at a later date.

The Government filing fee is calculated as follows:

Total claims	6	-	20	=	x	\$18.00	=	\$0.00
Independent claims	3	-	3	=	x	\$80.00	=	\$0.00
Base Fee								\$710.00
<b>TOTAL FEE</b>								<b>\$710.00</b>

A check for the statutory filing fee of \$710.00 is attached. You are also directed and authorized to charge or credit any difference or overpayment to Deposit Account No. 19-4880. The Commissioner is hereby authorized to charge any fees under 37 C.F.R. §§ 1.16 and 1.17 and any petitions for extension of time under 37 C.F.R. § 1.136 which may be required during the entire pendency of the application to Deposit Account No. 19-4880. A duplicate copy of this transmittal letter is attached.

Priority is claimed from November 26, 1999 based on Japanese Application No. 11-336763. The priority document will be filed at a later date.

Respectfully submitted,  
**SUGHRUE, MION, ZINN,**  
**MACPEAK & SEAS, PLLC**  
Attorneys for Applicant

By: J. Frank Osha  
J. Frank Osha  
Registration No. 24,625

1                   TITLE OF THE INVENTION

2                   **High Speed Timeslot Assignment Unit and Method for a TDMA**  
3                   **Communication System**

4                   BACKGROUND OF THE INVENTION

5                   Field of the Invention

6                   The present invention relates generally to TDMA or TDMA/TDD  
7                   (time division multiple access/time division duplex) wireless communication  
8                   systems, and more specifically to a timeslot assignment system and method  
9                   for a TDMA or TDMA/TDD wireless communication system.

10                  Description of the Related Art

11                  Fig. 1 illustrates a prior art timeslot assignment unit of a TDMA/TDD  
12                  cell-site station of a mobile communication network. The prior art timeslot  
13                  assignment unit includes a reception unit 10, a slot status memory 11, a  
14                  control data generation/sequence control (CDG/SC) unit 12 and an  
15                  assignment table 13. Reception unit 10 is arranged to receive information  
16                  indicating requirements, or assignment terms to be met for each timeslot to  
17                  be assigned. In response to an assignment request signal, the reception unit  
18                  10 accesses the status memory 11 to check to see if the timeslots requested can  
19                  be accommodated or not, and sends back a response to the requesting source  
20                  with an indication as to the check result. If all the requested timeslots can be  
21                  accommodated, the reception unit 10 sends an assignment command signal  
22                  to the CDG/SC unit 12. In response to the assignment command signal, the  
23                  CDG/SC unit 12 receives the assignment terms and produces therefrom a  
24                  plurality of control data and stores them into the assignment table 13, the  
25                  contents of which are used by a framing unit when a frame is formulated for

1 transmission. The control data stored in the assignment table 13 must be  
2 reordered in such a sequence that it conforms to the sequence in which  
3 frames are transmitted. However, the reordering is based on the memory  
4 swapping principle, and hence it requires a complex logic circuit. Because of  
5 the complex logic circuitry, the prior art timeslot assignment unit cannot  
6 operate at a high speed.

7 SUMMARY OF THE INVENTION

8 It is therefore an object of the present invention to provide a high  
9 speed timeslot assignment unit and method for TDMA or TDMA/TDD  
10 communication systems.

11 The high speed operation is attained by using pointer addressing  
12 instead of prior art memory swapping.

13 According to a first aspect, the present invention provides a slot  
14 assignment unit for use in a TDMA transmitter, which comprises first and  
15 second tables. A control data generation unit is provided for receiving  
16 assignment terms for a plurality of time slots and slot data from an external  
17 source, producing a set of assignment control data according to the  
18 assignment terms and the slot data and storing the set of assignment control  
19 data into an entry of the first table in response to a command signal applied  
20 thereto. A sequence controller analyzes a plurality of sets of assignment  
21 control data, produces a plurality of address pointers, and stores address  
22 pointers in the second table in such a sequence that the address pointers can  
23 be sequentially read out in a desired transmission sequence, and supplies the  
24 command signal to the control data generation unit in response to each of the  
25 address pointers.

1        According to a second aspect, the present invention provides a TDMA  
2 transmitter comprising a first table, a second table, a control data generation  
3 unit for receiving assignment terms for a plurality of time slots and slot data  
4 from an external source, producing a set of assignment control data according  
5 to the assignment terms and the slot data and storing the set of assignment  
6 control data into an entry of the first table in response to a command signal  
7 applied thereto. A sequence controller is provided for analyzing a plurality  
8 of sets of assignment control data, producing a plurality of address pointers,  
9 storing the address pointers in the second table in such a sequence that the  
10 address pointers can be sequentially read out from a starting address, and  
11 supplying the command signal to the control data generation unit in response  
12 to each of the address pointers. A framing unit sequentially reads address  
13 pointers from the starting address of the second table and reads assignment  
14 control data from entries of the first table specified by the read address  
15 pointers and formulates a frame with the read assignment control data.

16        According to a third aspect, the present invention provides a slot  
17 assignment method for a TDMA transmitter, comprising the steps of (a)  
18 receiving assignment terms for a plurality of time slots, (b) producing a set of  
19 assignment control data according to the assignment terms, (c) repeating  
20 steps (a) and (b) to produce a plurality of sets of assignment control data, (d)  
21 analyzing said plurality of sets of assignment control data, (e) storing one of  
22 said sets of assignment control data into an entry of a first table, (f) storing an  
23 address pointer in a second table corresponding to said entry of said first  
24 table, and (g) repeating steps (d) to (f) until all assignment control data are  
25 stored in the first table. The slot assignment method may further includes the

1 steps of sequentially reading address pointers from a starting address of the  
2 second table and reading assignment control data from the first table in  
3 accordance with the read address pointers, and formulating a frame with the  
4 read assignment control data.

5                   BRIEF DESCRIPTION OF THE DRAWINGS

6                   The present invention will be described in detail further with reference  
7 to the following drawings, in which:

8                   Fig. 1 is a block diagram of a prior art slot assignment unit of a  
9 TDMA/TDD cell-site station;

10                  Fig. 2 is a block diagram of a TDMA/TDD cell-site system in which the  
11 timeslot assignment unit of the present invention is incorporated;

12                  Fig. 3 is a block diagram of the slot assignment unit of the present  
13 invention; and

14                  Fig. 4 is a flowchart of the operation of a sequence controller according  
15 to the present invention.

16                   DETAILED DESCRIPTION

17                  Referring now to Fig. 2, there is shown a transceiver that can be used  
18 in a demand-assigned dynamic TDMA (time division multiple access) system  
19 or a dynamic TDMA/TDD (time division multiple access/time division  
20 duplex) system in which a TDMA frame is segmented into timeslots (or  
21 simply slots) and transmit/receive unit data, or packets (such as data packets  
22 and control packets) are assigned to a plurality of slots and scheduled on an  
23 on-demand basis. The transceiver is particularly designed to be used as a  
24 cell-site station of a TDMA cellular mobile communication network.

25                  The TDMA/TDD scheduling and framing functions of a cell-site

1 station is embodied in the transceiver of Fig. 2, in which the cell-site station is  
2 comprised of a slot assignment unit 21, a TDMA/TDD framing unit 22 to  
3 which a modem 29 is connected, a memory controller 13 with which a data  
4 memory 24 is associated, a CPU 25, a ROM 26 and a RAM 27, all of which are  
5 connected to a common bus 28. CPU 25 operates according to a programmed  
6 routine stored in the ROM 16 to perform memory control, TDMA/TDD  
7 scheduling, framing and slot assignment control. RAM 27 serves as a work  
8 area for data to be processed by the CPU 25. Data memory 24 is accessed by  
9 the memory controller 23 to store data to be transmitted to or received from  
10 mobile terminals via the framing unit 22.

11       CPU 25 constantly monitors the contents of the data memory 24 via the  
12 memory controller. When a data packet or a control packet is stored in the  
13 data memory 24, the CPU 25 determines the size of the packet, the address of  
14 the packet in the data memory 24, the packet type, and the destination  
15 address and produces an assignment request signal containing these items of  
16 slot data. CPU 25 further produces information regarding the requirements  
17 or assignment terms to be met for each time slot to be assigned. The  
18 assignment terms information include priority levels classified according to  
19 communication services and urgency, type of packets, and uplink-to-  
20 downlink ratio within the frame.

21       As shown in detail in Fig. 3, the slot assignment unit 21 is comprised of  
22 a reception unit 30, a status memory 31, a control data generation (CDG) unit  
23 32, a control data table 33, a sequence controller 34 and an address pointer  
24 table 35.

25       From the CPU 25, the reception unit 30 receives the assignment

1 request signal and the assignment terms signal. In response to the  
2 assignment request signal, the reception unit 30 calculates the number of slots  
3 that can be assigned to TDMA frames based on data contained in the request  
4 signal as well as on the assignment terms and accesses the status memory 31  
5 to check to see if the determined slots can be accommodated or not by the  
6 currently available slots, and sends back a response to the CPU 25 indicating  
7 the result of the check.

8 If all the requested slots can be accommodated, the reception unit 30  
9 sends an assignment command signal to the CDG unit 32. In response to the  
10 command signal, the CDG unit 32 receives the assignment request signal and  
11 the assignment terms signal from the reception unit 30. By using the  
12 assignment terms, the CDG unit 32 produces a set of assignment control data  
13 for the assignment unit (ten slots, for example) and produces a plurality of  
14 sets of assignment control data by repeatedly receiving assignment request  
15 signals. CDG unit 32 holds the sets of assignment control data until it  
16 receives a transfer command signal from the sequence controller 34 for each  
17 entry of the control data table 33.

18 Each set of assignment control data includes data type, mobile  
19 address, communication mode, starting address of slots in the data memory  
20 24, the number of slots contained in an assignment unit, the address of the  
21 assigned slot in the data memory 24 and ancillary data. When each set of  
22 assignment control data is produced, the CDG unit 32 updates the slot status  
23 memory 31. When the slot status memory 31 is overflowed, assignment  
24 request from the CPU 25 will be rejected. For each assignment request from  
25 the CPU 25, a set of assignment control data is stored in one entry of the

1 control data memory 33.

2 Sequence controller 34 responds to the start timing signal from the  
3 framing unit 22 by analyzing a plurality of sets of assignment control data  
4 maintained in the CDG unit 32 and sequentially produces address pointers  
5 according to the TDMA slot assignment rule, indicating the addresses of the  
6 entries of the control data table 33. The address pointers are stored into an  
7 address pointer table 35 such that corresponding assignment control data are  
8 read out from the control data table 33 in the same sequence as time slots are  
9 transmitted from the cell-site station. Address pointer table 35 may be  
10 implemented in a configuration similar to a shift register in which stored  
11 address pointers are automatically shifted when a new address pointer is  
12 stored if the storage location of the new pointer is ahead of, or in between, the  
13 previously stored pointers.

14 As shown in Fig. 4, the write operation of the sequence controller 34  
15 starts with decision step 41 when the start timing signal is received from the  
16 framing unit 22 and analyzes a plurality of sets of assignment control data  
17 maintained in the CDG unit 32 (step 42). At step 43, the sequence controller  
18 34 supplies a transfer command signal to the CDG unit 32 to transfer its  
19 assignment control data into the first entry of the slot data table 33 and  
20 produces a corresponding address pointer and stores it in the first entry of  
21 the address pointer table 35 (step 44). If all assignment control data of the  
22 current assignment unit have been stored (step 45), the sequence controller 34  
23 terminates the routine. If not, the sequence controller 34 returns to step 42 to  
24 repeat the same process until all assignment control data of the assignment  
25 unit are stored in the control data table 33 with their corresponding address

1    pointers in the address table 35. Therefore, steps 42 to 45 are repeatedly  
2    performed a number of times corresponding in number to assignment  
3    request signals received from the CPU 25.

4       When a frame is formulated, the framing unit 22 sequentially reads  
5    address pointers from the starting address of the address pointer table 35.  
6    Using the read address pointers, the framing unit reads the contents of the  
7    control data table 32 and inserts transmit data into assigned slots of the frame  
8    for transmission.

What is claimed is:

1. A slot assignment unit for use in a time division multiple access (TDMA) transmitter, comprising:
  3. a first table;
  4. a second table;
  5. a control data generation unit for receiving assignment terms for a plurality of time slots and slot data from an external source, producing a set of assignment control data according to the assignment terms and the slot data and storing the set of assignment control data into an entry of said first table in response to a command signal applied thereto; and
  10. a sequence controller for analyzing a plurality of said sets of assignment control data, producing a plurality of address pointers, storing said plurality of address pointers in said second table in such a sequence that the address pointers can be sequentially read out in a desired transmission sequence, and supplying said command signal to said control data generation unit in response to each of said address pointers.
1. The slot assignment unit of claim 1, wherein said TDMA transmitter includes a data memory for storing a plurality of transmit data, and wherein said set of assignment control data stored in said first table includes an address of a communication terminal, a starting address point of each transmit data in said data memory, and a count number of slots assigned to said entry.
1. 3. A time division multiple access (TDMA) transmitter

2 comprising:

3       a first table;

4       a second table;

5       a control data generation unit for receiving assignment terms for a

6       plurality of time slots and slot data from an external source, producing a set

7       of assignment control data according to the assignment terms and the slot

8       data and storing the set of assignment control data into an entry of said first

9       table in response to a command signal applied thereto; and

10      a sequence controller for analyzing a plurality of said sets of

11     assignment control data, producing a plurality of address pointers, storing

12     said plurality of address pointers in said second table in such a sequence that

13     the address pointers can be sequentially read out from a starting address of

14     the second table, and supplying said command signal to said control data

15     generation unit in response to each of said address pointers;

16      a data memory for storing a plurality of transmit data; and

17      a framing unit for sequentially reading address pointers from said

18     starting address of said second table and reading assignment control data

19     from entries of said first table which are specified by the read address

20     pointers and formulating a frame with the read assignment control data and

21     said plurality of transmit data from said data memory.

1       4.      The TDMA transmitter of claim 3, wherein said set of

2     assignment control data stored in said first table includes an address of an

3     assigned communication terminal, a starting address point of each transmit

4     data in said data memory, and a count number of assigned slots.

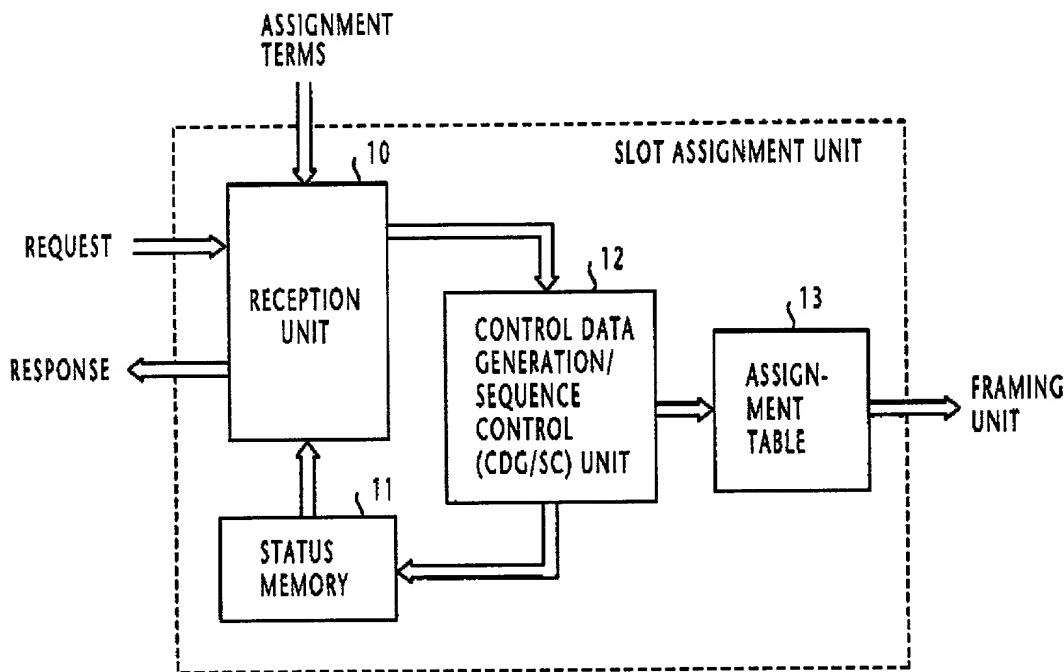
1        5. A slot assignment method for a time division multiple access  
2 (TDMA) transmitter, comprising the steps of:  
3            a) receiving assignment terms for a plurality of time slots and slot  
4 data;  
5            b) producing a set of assignment control data according to the  
6 assignment terms and the slot data;  
7            c) repeating steps (a) and (b) to produce a plurality of sets of  
8 assignment control data;  
9            d) analyzing said plurality of sets of assignment control data;  
10          e) storing one of said sets of assignment control data into an entry  
11 of a first table;  
12          f) storing an address pointer in a second table corresponding to  
13 said entry of said first table; and  
14          g) repeating steps (d) to (f) until all of said assignment control data  
15 are stored in the first table.

1        6. The slot assignment method of claim 5, further comprising the  
2 steps of:  
3            sequentially reading address pointers from a starting address of said  
4 second table and reading said plurality of sets of assignment control data  
5 from said first table in accordance with the read address pointers; and  
6            formulating a frame with the assignment control data read from the  
7 first table.

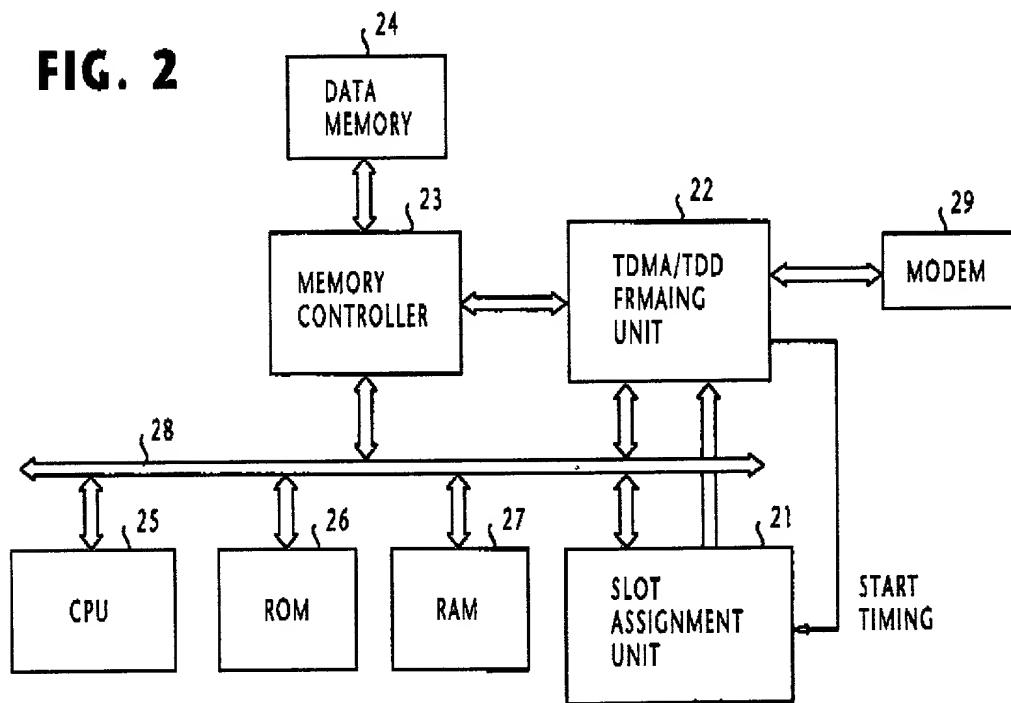
ABSTRACT OF THE DISCLOSURE

1        In a TDMA/TDD transmitter, a control data generation unit receives  
2 assignment terms for a number of time slots and slot data from an external  
3 source, produces a set of assignment control data according to the assignment  
4 terms and the slot data and stores the set of assignment control data into an  
5 entry of a control data table in response to a transfer command signal. A  
6 sequence controller analyzes sets of assignment control data maintained in  
7 the control data generation unit and produces a number of address pointers.  
8 The address pointers are stored in an address pointer table in such a sequence  
9 that they can be sequentially read out in a desired transmission sequence.  
10 The aforesaid transfer command signal is supplied from the sequence  
11 controller to the control data generation unit in response to each of the  
12 address pointers. A framing unit sequentially reads address pointers from  
13 the starting address of the address pointer table, reads assignment control  
14 data from the control data table in accordance with the read address pointers,  
15 and formulates a frame. Transmit data stored in a data memory is inserted  
16 into the frame for transmission.

**FIG. 1**  
PRIOR ART

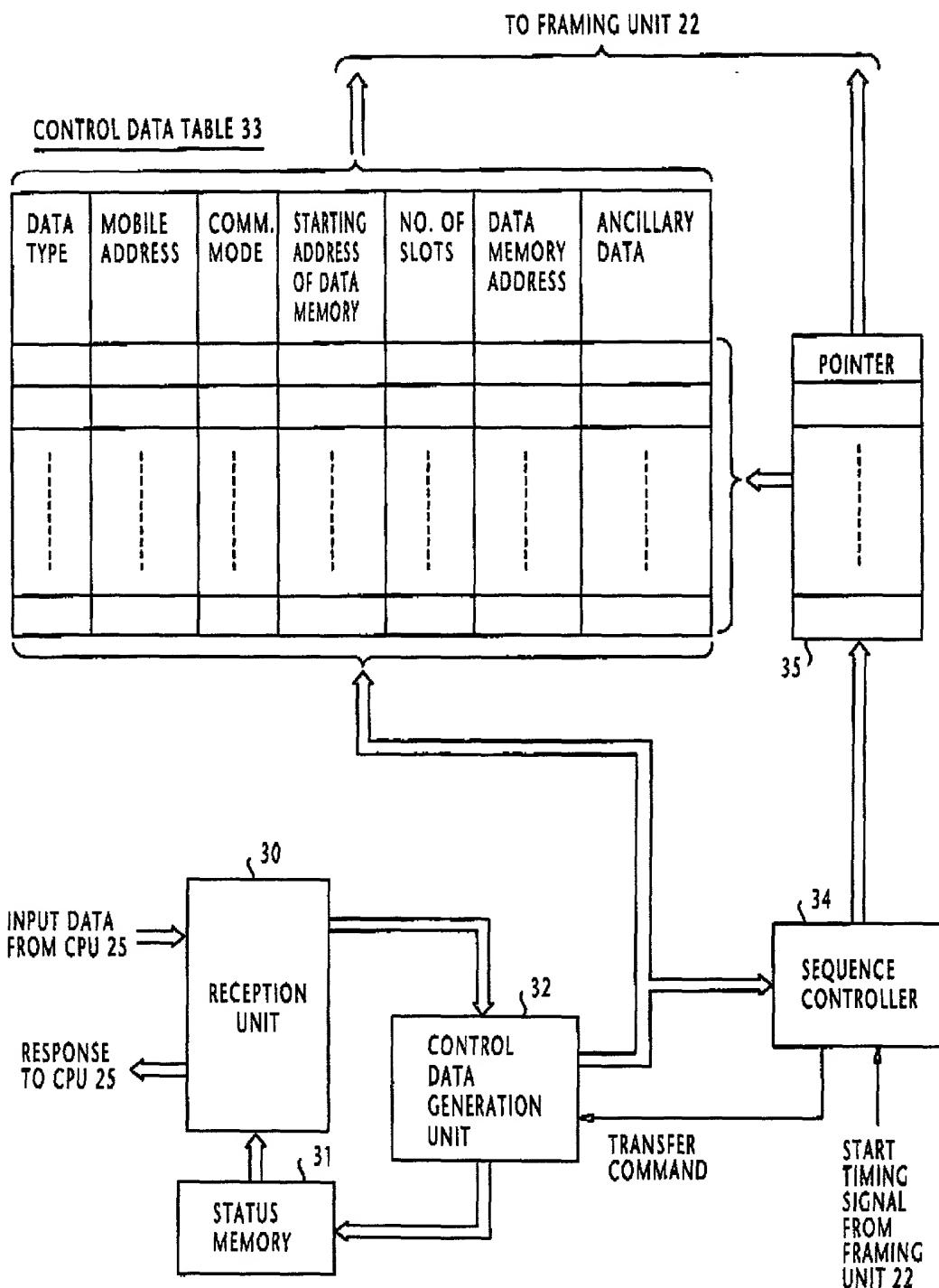


**FIG. 2**

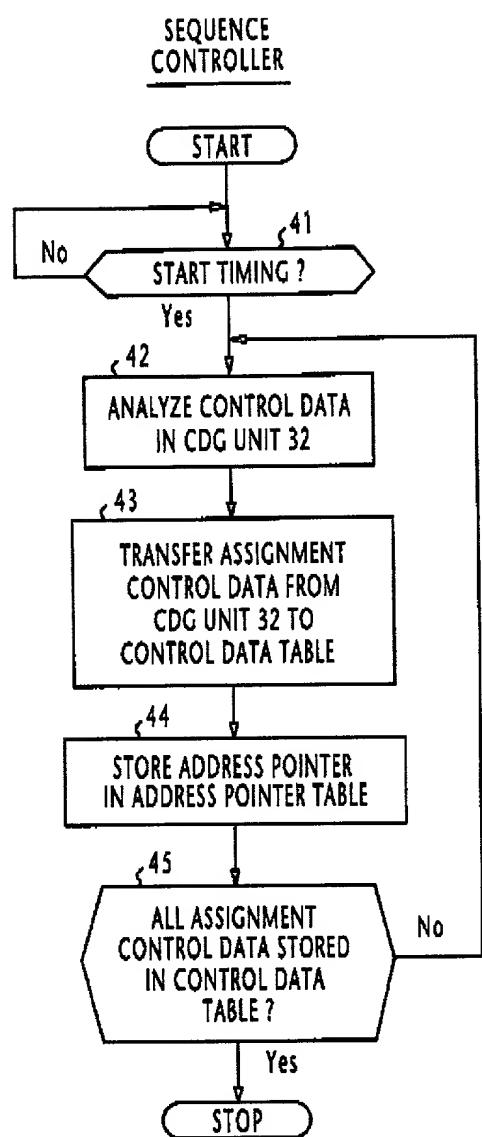


**FIG. 3**

**SLOT ASSIGNMENT UNIT 21**



**FIG. 4**



## DECLARATION AND POWER OF ATTORNEY

日本特許出願

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name; that I verily believe I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural names are listed below) of the subject matter claimed and for which a patent is sought in the application entitled:

High Speed Timeslot Assignment Unit and Method for  
a TDMA Communication System.

which application is:

the attached application  
(for original application)

application Serial No. \_\_\_\_\_  
filed \_\_\_\_\_, and amended on  
\_\_\_\_\_

(for declaration not accompanying application)

that I have reviewed and understand the contents of the specification of the above-identified application, including the claims, as amended by any amendment referred to above; that I acknowledge my duty to disclose information of which I am aware which is material to the patentability of this application under 37 C.F.R. 1.56, that I hereby claim foreign priority benefits under Title 35, United States Code §119, §172 or §365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified on said list any foreign application for patent or inventor's certificate on this invention having a filing date before that of the application on which priority is claimed:

Application Number	Country	Filing Date	Priority Claimed (yes or no)
11-336763	Japan	November 26, 1999	Yes

I hereby claim the benefit of Title 35, United States Code §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in a listed prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge my duty to disclose any information material to the patentability of this application under 37 C.F.R. 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application Serial No.	Filing Date	Status (patented, pending, abandoned)
------------------------	-------------	--

I hereby appoint John H. Mion, Reg. No. 18,879; Donald E. Zinn, Reg. No. 19,046; Thomas J. Macpeak, Reg. No. 19,292; Robert J. Seas, Jr., Reg. No. 21,092; Darryl Mexic, Reg. No. 23,063; Robert V. Sloan, Reg. No. 22,775; Peter D. Olexy, Reg. No. 24,513; J. Frank Osha, Reg. No. 24,625; Waddell A. Biggart, Reg. No. 24,861; Robert G. McMorrow, Reg. No. 19,093; Louis Gubinsky, Reg. No. 24,835; Neil B. Siegel, Reg. No. 25,200; David J. Cushing, Reg. No. 28,703; John R. Inge, Reg. No. 26,916; Joseph J. Ruch, Jr., Reg. No. 26,577; Sheldon I. Landsman, Reg. No. 25,430; Richard C. Turner, Reg. No. 29,710; Howard L. Bernstein, Reg. No. 25,665; Alan J. Kasper, Reg. No. 25,426; Kenneth J. Burchfiel, Reg. No. 31,333; Gordon Kit, Reg. No. 30,764; Susan J. Mack, Reg. No. 30,951; Frank L. Bernstein, Reg. No. 31,484; Mark Boland, Reg. No. 32,197; William H. Mandir, Reg. No. 32,156; Scott M. Daniels, Reg. No. 32,562; Brian W. Hannon, Reg. No. 32,778 and Abraham J. Rosner, Reg. No. 33,276, my attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith, and request that all correspondence about the application be addressed to SUGHRUE, MION, ZINN, MACPEAK & SEAS, 2100 Pennsylvania Avenue, N.W., Washington, D.C. 20037-3202.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 101 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date November 22, 2000

First Inventor Junichi

First Name Middle Initial Last Name



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